



Panipat Institute of Engineering and Technology

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Department of Electronics and Communication Engineering

Ref. No-PIET/ECE/ICT/2021/02

Date: 13th April, 2021

NOTICE

The Department of Electronics & Communication Engineering, PIET will organize event on
“**Chip Design and Failure Analysis**” on 17th April 2021 on the Zoom platform from 12:30 pm-2
p.m. The link will be shared 30 minutes before commencement of session in whatsapp groups.


Department of ECE
Panipat Institute of Engineering & Technology
Samalkha-132102, Panipat
Ms. Swati Gupta
Head of Department

Cc:
Notice boards



Report on Event on Chip Design and Failure Analysis

Event Title: “Chip Design and Failure Analysis”

Date & Time: 17th April 2021, 12:30 pm

Mode of Activity: Online

Resource Person (if any): Mr. Sanchit Garg, Failure Analysis Engineer at Intel Corporation, USA. Contact no. +1(480)307-7260

Coordinator : Dr. Monika Gambhir Associate Prof. ECE department & Mr. Vishal Jain A.P ECE department.

Organized by: Department of ECE

Department of Electronics & Communication Engineering organized an expert talk on Chip Design and Failure Analysis. Ms. Swati Gupta Head, ECE department welcomed resource person Mr. Sanchit Garg, Failure Analysis Engineer. Then Dr. Monika Gambhir introduced the resource person and gave a brief introduction of Microprocessors. Mr. Sanchit Garg provided a comprehensive overview of semiconductor technology and chip design. He discussed the design flow from specification to fabrication, emphasizing the importance of each stage in creating efficient chips. The objective of event was to discuss how chip design and failure analysis is carried out at Intel, USA and to share the job opportunities in VLSI design field. The outcome of the seminar was a well-rounded enhancement of the students' academic and professional capabilities, positioning them for success in the ever-evolving field of electronics and communication engineering.

About expert:

Mr. Sanchit Garg, Failure Analysis Engineer at Intel Corporation, USA was the expert of the event. He has 3 years of experience in chip failure analysis. He delivered a wonderful event on the topic and sorted all the queries of the students regarding working in VLSI design domain.

45 students and 10 faculty members participated in the event. Participants were introduced to industry-standard tools such as Cadence, Synopsys, and Mentor Graphics. The event included setting up the design environment and understanding

basic functions essential for chip design The event concluded by vote of thanks delivered by coordinator Ms. Sapna Arora.

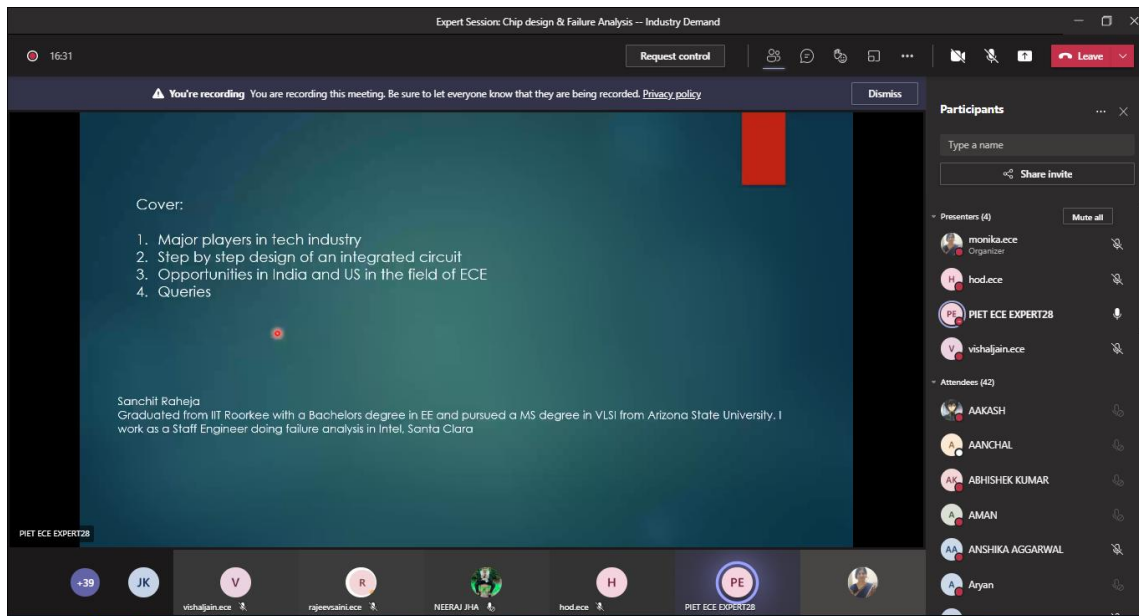


Photo1:Screenshot depicting the contents to be covered in Lecture

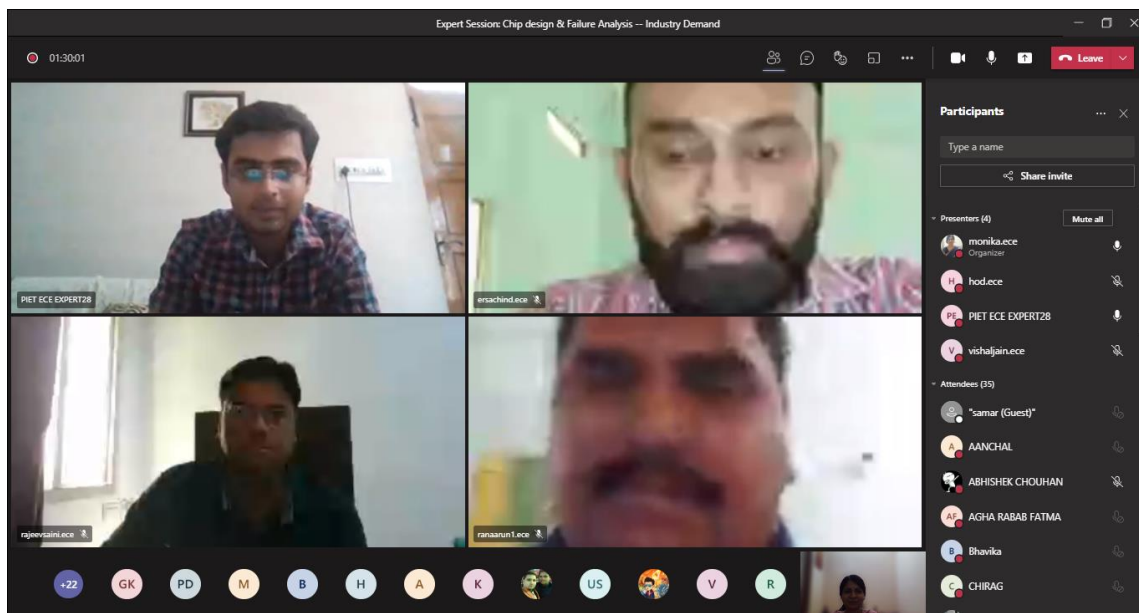


Photo 2: Mr. Sanchit Garg interacting with participants



PANIPAT INSTITUTE OF ENGINEERING AND TECHNOLOGY

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"Chip design & failure Analysis"

List of attendees

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Mr. Vishal Jain

A.P, ECE department.