PANIPAT INSTITUTE OF ENGINEERING & TECHNOLOGY
Department of Electronics & Communication Engineering

LESSON PLAN

Subject Name: - Verilog HDL **Subject Code: - EC-306A**
Year: - 3rd **Semester:-6th**

Lecture No	Unit No	Topic	References
L 1	1	Introduction, conventional approach to digital design, VLSI design	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons.
L 2	1	ASIC design flow, Role of HDL.Conventional Data flow, ASIC data flow,	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 3	1	Verilog as HDL, Levels of Design Description	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 4	1	Concurrency, Simulation and Synthesis, Functional Verification, System Tasks	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 5	1	Programming Language Interface (PLI), Module, Simulation and Synthesis Tools, Test Benches	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 6	1	Language constructs and conventions: Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers,	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons

		Strings	
L 7	1	Logic Values, Strengths,	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 8	1	Data Types, Scalars and Vectors	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 9	1	Parameters, Memory, Operators, System Tasks	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 10	2	Gate level modeling: Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 11	2	Tri-State Gates, Array of Instances of Primitives, Additional Examples	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 12	2	Design of Flip-flops with Gate Primitives	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 13	2	Delays, Strengths and Contention Resolution, Net Types	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 14	2	Design of Basic Circuits	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 15	2	Behavioral modeling: Introduction, Operations and Assignments, Functional Bifurcation, Initial Construct, Always Construct, Examples, Assignments with Delays	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L16	2	Wait construct, Multiple Always Blocks,	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons

L 17	2	Designs at Behavioral Level	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 18	2	Blocking Assignments	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 19	2	Non-blocking Assignments	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 20	2	The case statement, Simulation Flow, if and ifelse Constructs	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 21	2	Assign-deassign construct, repeat construct,	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 22	2	for loop	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 23	2	The disable construct, while loop, forever loop	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 24	2	Parallel blocks, force-release construct, Event	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 25	3	Modeling at data flow level: Introduction, Continuous Assignment Structures,	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 26	3	Delays and Continuous Assignments	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 27	3	Assignment to Vectors, Operators,	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 28	3	Additional Examples	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 29	3	Switch level modeling: Introduction, Basic	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through*

		Transistor Switches	*Verilog HDL*. John Wiley & Sons
L 30	3	CMOS Switch,	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 31	3	Bi-directional Gates,	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 32	3	Time Delays with Switch Primitives	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 33	3	Instantiations with Strengths and Delays	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 34	3	Strength Contention with Trireg Nets	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 35	4	Functions, tasks, and user defined primitives: Introduction, Function, Tasks	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 36	4	User- Defined Primitives (UDP)	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 37	4	FSM Design (Moore Machines)	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L 38	4	FSM Design (Mealy Machines)	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L-39	4	System tasks, functions, and compiler directives: Introduction, Parameters, Path Delays	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L-40	4	Module Parameters	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L-41	4	System Tasks and	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through*

		Functions	*Verilog HDL*. John Wiley & Sons
L-42	4	File-Based Tasks and Functions	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L-43	4	Compiler Directives	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons
L-44	4	Hierarchical Access	Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons

Text Books:

1) Padmanabhan, T.R. and Sundari, B.B.T., 2003. *Design Through Verilog HDL*. John Wiley & Sons