Panipat Institute of Engineering & Technology
Department of CSE-AI&DS
LESSON PLAN

Subject: Computer Architecture **Subject code:** PC-CS-AIDS-309A
Semester: 5th

S.No	Topic	CO Covered	Assignment No.	Teaching Methodology
1	Unit 1: Introduction to Computer System	CO1	Assignment No.1	Board
2	Computer Organization and Architecture, Von neumann Architecture, Evolution and Computer generations			Board
3	Fixed point and floating-point number representation			Board
4	Digital arithmetic algorithm for addition.			Video
5	Booth ‘s Algorithm for subtraction.			PPT
6	Booth ‘s Algorithm for multiplication			Board
7	Booth ‘s Algorithm for division restoring method.			Board
8	Booth ‘s Algorithm for division Non restoring method.			Board
9	Memory Hierarchy, Main Memory and Auxiliary memory			Board
10	Unit 2: Instruction codes and stored program organization, computer register	CO2	Assignment No.2	Board
11	Common bus system, computer instruction and timing control			Board
12	Instruction cycle, register reference instruction, memory reference instructions			Board
13	Input, output and interrupt: configuration, Instructions, program interrupt			PPT & Board
14	Interrupt cycle, microprogrammed control organization, control memory, address sequencing			Board
15	Microinstruction format, horizontal vs vertical micro programming			Board
16	Revision of Unit-2			Flip Learning
17	Unit-3 General register organization,			Board
18	Stack Organization			Board
19	Instruction Formats			Board
20	Addressing modes			Flip Learning
21	Addressing modes	CO3	Assignment No.-3	Board
22	Data transfer and manipulation			Board

23	Program control			Board
24	CISC and RISC, features and comparison			Video
25	Pipeline and vector processing			Board
26	Parallel processing			Board
27	Flynn's taxonomy			Board
28	Pipelining instruction pipeline			Board
29	Basics of vector processing			Board
30	Array processor			PPT
31	Numerical on addressing modes			PPT
32	Revision of Unit-3			Flip Learning
33	Unit 4: I/O interface, I/O Bus and interface module			PPTS
34	I/O versus memory bus	CO4	Assignment No.4	PPTS
35	Asynchronous data transfer: strobe control			PPTS
36	Handshaking, Asynchronous serial transfer			PPTS
37	Modes of transfer, Programmed I/Interrupt driven I/O, Priority interrupt			PPTS
38	Daisy chaining, parallel priority interrupt			PPTS
39	DMA, Input/output processor, serial communication			PPTS