PANIPAT INSTITUTE OF ENGINEERING & TECHNOLOGY
Department Of Computer Science & Engineering
LESSON PLAN

Semester: 5th

Course Title: Computer Organization & Architecture

Course No. PC-CS-307A

Sr. No.	Lecture No	Topics to be covered
1	L-1	**Unit 1: Data representation and computer arithmetic :**Introduction to computer Systems
2	L-2	Organization and architecture, Von Neumann Architecture
3	L-3	Evolution and computer generations
4	L-4	Fixed point representation of numbers
5	L-5	Digital arithmetic algorithms for Addition, Subtraction
6	L-6	Multiplication using Booth's algorithm
7	L-7	Division by using restoring and non-restoring algorithms
8	L-8	Floating point representation with IEEE standards and its arithmetic operations.
9	L-9	Memory Organization: Memory Hierarchy, Main Memory, Auxiliary Memory
10	L-10	Associative Memory, Cache Memory, Virtual Memory
11	L-11	**Cache Coherence and Synchronization Mechanisms (Beyond curriculum)**
12	L-12	Revision of Unit topics
13	L-13	**Unit: Basic Computer organization and Design**: Instruction codes, Stored program organization
14	L-14	Computer registers and common bus system
15	L-15	Computer instructions, timing and control
16	L-16	Instruction cycle: Fetch and Decode, Register reference instructions; Memory reference instructions
17	L-17	Input, output and Interrupt: configuration, instructions
18	L-18	Program interrupt, Interrupt cycle
19	L-19	Micro programmed Control organization

20	L-20	Control Memory, address sequencing
21	L-21	Micro program Example, micro instruction format
22	L-22	Horizontal Vs Vertical micro-programming, design of Control unit
23	L-23	Micro-program sequencer, Hardwired v/s Micro-Programmed Control unit
24	L-24	Revision of Unit 2 topics
25	L-25	**Unit 3: Central Processing Unit**: General register organization, Stack organization
26	L-26	Instruction formats (Zero, One, Two and Three Address Instruction)
27	L-27	Addressing modes
28	L-28	Data transfer and manipulation, Program control
29	L-29	CISC and RISC: features and comparison
30	L-30	Pipeline and vector Processing
31	L-31	Parallel Processing, Flynn's taxonomy
32	L-32	Pipelining, Instruction Pipeline
33	L-33	Basics of vector processing and Array Processors
34	L-34	**Emergence of superscalar processors (Beyond curriculum)**
35	L-35	Revision of Unit3 topics
36	L-36	**Unit4: Input-output organization:** I/O interface, I/O Bus and interface modules
37	L-37	I/O versus Memory Bus
38	L-38	Asynchronous data transfer: Strobe control, Handshaking
39	L-39	Asynchronous serial transfer
40	L-40	Modes of Transfer: Programmed I/O, Interrupt driven I/O
41	L-41	Priority interrupt, Daisy chaining, Parallel Priority interrupt
42	L-42	Direct memory Access, DMA controller and transfer
43	L-43	Input output Processor
44	L-44	CPU-IOP communication, Serial communication
45	L-45	Revision of Unit 4 topics