PANIPAT INSTITUTE OF ENGINEERING & TECHNOLOGY
Department of Electronics & Communication Engineering

LESSON PLAN

Subject Name: - Computer Organization and Architecture **Subject Code: EC-305A**
Year: - 3rd **Semester: - 5th**

Lecture No	Unit No	Topic	References
L 1	UNIT-I	Introduction to basic computer architecture	Morris Mano, "Computer System Architecture", PHI.
L 2		Register transfer	
L 3		Bus and memory transfers	
L 4		Arithmetic, logic and shift micro-operations	
L 5		Central Processing Unit: Introduction, general register organization	
L 6		Stack organization	
L 7		Instruction formats, addressing modes	
L 8		Data transfer and manipulation, Program control	
L 9		RISC, Macros and Subroutines	
		Revisions	
L 10	UNIT-II	Micro programmed control, control memory	J.F. Heys, "Computer Organization and Architecture", TMH.
L 11		Address sequencing, micro program example, design of control unit	
L 12		Hardwired Control: Design methods, Multiplier Control Unit, CPU Control unit.	
L 15		Processor Design: Decimal arithmetic unit –BCD adder, BCD subtraction, decimal arithmetic operations	J. Hennessy and D. Patterson, Computer Architecture a Quantitative Approach, 3rd Ed, Morgan Kaufmann, 2002.
L16		Forms of Parallel processing classification of Parallel structures	
L17		Array Processors, Structure of general-purpose Multiprocessors	
L 20		Revisions	
L 21	UNIT-III	Memory hierarchy	J.F. Heys, "Computer Organization and Architecture", TMH
L 22		Device characteristics	
L 23		Auxiliary memory	
L 24		Associative memory	
L 25		Cache memory	

L 26		Virtual memory	
L 27		Memory management	
L 28		Hardware multiprocessor architectures and their characteristics, interconnection structures	
L 29		Semiconductor RAMS, Serial-access Memories – Memory organization, Main Memory Allocation	
L 30	UNIT-IV	Parallel processing, Pipelining,	Morris Mano, "Computer System Architecture", PHI.
L 31		Arithmetic pipeline, Instruction pipeline	
L 32		RISC pipeline	
L 33		Vector processing, array processors	
L 34		Input-output Organization: Peripheral devices, input- output interface	
L 35		Asynchronous data transfer	
L 36		Modes of transfer	
L37		Priority interrupt	
L38		DMA	
L39		Revision	

Textbooks:

1. Morris Mano, "Computer System Architecture", PHI.
2. J.F. Heys, "Computer Organization and Architecture", TMH.

Reference Books:

1. J. Hennessy and D. Patterson, Computer Architecture A Quantitative Approach, 3rd Ed, Morgan Kaufmann, 2002.