# PANIPAT INSTITUTE OF ENGINEERING AND TECHNOLOGY
# PANIPAT
# DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

## LESSON PLAN

**Subject Name: -Digital Electronics**
**Branch/Semester: -3rd Sem**
**Subject Code:-ES-207A**

| Sr. No. | Lecture No. | Topics To Be Covered |
|---|---|---|
| 1. | L1 | Unit-1: Introduction of Digital Electronics |
| 2. | L2 | Some basics of Number System |
| 3. | L3 | Logic Gates: AND, OR, NOT, NAND, NOR |
| 4. | L4 | Exclusive-OR and Exclusive NOR gates |
| 5. | L5 | Implementation of Logic Functions using gates |
| 6. | L6 | NAND- NOR Implementation |
| 7. | L7 | Gate Multilevel Implementation |
| 8. | L8 | Boolean Postulates |
| 9. | L9 | Laws of Boolean algebra |
| 10. | L10 | De-Morgan's Theorem, |
| 11. | L11 | Principle of duality and Boolean Expression Simplification |
| 12. | L12 | Minterms, Maxterms, SOP, POS |
| 13. | L13 | K-map techniques |
| 14. | L14 | K Map minimization problems |
| 15. | L15 | Quine -Mccluskey method on SOP question |
| 16. | L16 | Q M method on POS, don’t care condition |
| 17. | L17 | Q M method questions |
| 18. | L18 | TTL with NAND gate |
| 19. | L19 | CMOS with NAND & its characteristics |
| 20. | L20 | **Unit-2**: Half Adder & Full Adder |
| 21. | L21 | Half Subtractor & Full Subtractor |
| 22. | L22 | Parallel Binary Adder, Parallel Binary Subtractor |
| 23. | L23 | Fast & Carry Look Ahead Adder, |
| 24. | L24 | Serial Adder/Subtractor |
| 25. | L25 | BCD adder/Subtractor |
| 26. | L26 | Decoder, |
| 27. | L27 | Encoder |
| 28. | L28 | Multiplexer Description |
| 29. | L29 | Demultiplexer Description |
| 30. | L30 | Demultiplexer |
| 31. | L31 | Parity Generator and checker |

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| 32. | L32 | Test |
| 33. | L33 | **Unit 3**:Flip flop and latch concept |
| 34. | L34 | Edge Triggering, Level Triggering, |
| 35. | L35 | Realization of Flip-Flop using other flip-flops. |
| 36. | L36 | Serial adder, subtractor, |
| 37. | L37 | Asynchronous Ripple or serial counter |
| 38. | L38 | UP/Down Counter |
| 39. | L39 | Synchronous Counter |
| 40. | L40 | Synchronous up/down counter |
| 41. | L41 | Programmable Counters, |
| 42. | L42 | Design of Synchronous Counter |
| 43. | L43 | State diagram description |
| 44. | L44 | State table, state minimization |
| 45. | L45 | State assignment |
| 46. | L46 | Excitation table |
| 47. | L47 | Maps implementation |
| 48. | L48 | Modulo-n counter ,shift registers, Universal shift register |
| 49. | L49 | 555 timer, shift registers introduction |
| 50. | L50 | Types of shift registers, Shift register counter |
| 51. | L51 | Ring counter, Sequence generator |
| 52. | L52 | **Unit-4**: Classification of Memories: RAM, ROM, PROM, EPROM, EEPROM, EAPROM |
| 53. | L53 | RAM organization, Write operation, Read operation, Memory cycle, Timing waveforms |
| 54. | L54 | A/D Convertors |
| 55. | L55 | D/A Convertors |
| 56. | L56 | Memory decoding, memory expansion, Static and bipolar RAM cells MOSFET RAM cells, Dynamic RAM Cells |
| 57. | L57 | Programmable Logic devices (PLA), PAL. |
| 58. | L58 | PLA using ROM |
| 59. | L59 | Revision |