PANIPAT INSTITUTE OF ENGINEERING AND TECHNOLOGY
PANIPAT
DEPARTMENT OF CYBER SECURITY
LESSON PLAN

Subject: MICROPROCESSOR & INTERFACING Subject CodeES-CS-CYS-307A
Semester:5th

Sr. No.	Lecture No.	Topics To Be Covered	Mode of Delivery
1	L 1	Unit: 1 8086 CPU Architecture	Class Room
2	L 2	8086 Block diagram; Description of data registers, address registers; pointer and index registers, Queue, BIU and EU.	Smart Class Room
3	L 3	PSW	Class Room
4	L 4	8086 Pin diagram description	Class Room
5	L 5	Generating 8086 CLK and reset signals using 8284. WAIT state generation	Smart Class Room
6	L 6	Microprocessor BUS types and buffering techniques	Class Room
7	L 7	8086 Minimum mode module	Smart Class Room
8	L 8	Maximum mode CPU module	Class Room
9	L 9	8086 CPU Read/Write timing diagrams in minimum mode and maximum mode	Class Room
10	L 10	Address decoding techniques. Interfacing SRAMS; ROMS/PROMS	Class Room
11	L 11	Address decoding techniques. Interfacing SRAMS; ROMS/PROMS	Class Room
12	L 12	Interfacing and refreshing DRAMS.	Class Room
13	L 13	Unit: 3 8086 Instruction Set: Instruction formats,	Class Room
14	L 14	Addressing modes	Smart Class Room
15	L 15	Data transfer instructions	Class Room
16	L16	String instructions, logical instructions	Smart Class Room
17	L 17	Arithmetic instructions	Class Room
18	L 18	Transfer of control instructions; process control instructions	Smart Class Room
19	L 19	Assembler directives	Class Room

20	L 20	Unit-4 Basic I/O Interface: Parallel and Serial I/O Port design and address decoding.	Class Room
21	L 21	Intel's 8255 description and interfacing with 8086	Class Room
22	L 22	Intel's 8255 description and interfacing with 8086	
23	L 23	ADCs - types, operation and interfacing with 8086	Class Room
24	L 24	DACs - types, operation and interfacing with 8086	Class Room
25	L 25	Interfacing of Keyboards, alphanumeric displays	Class Room
26	L 26	Interfacing of multiplexed displays	Class Room
27	L 27	Interfacing of stepper motor	Class Room
28	L28	Memory mapped I/O Vs Isolated I/O	Class Room
28	L 28	Interfacing of optical encoder with 8086	Class Room
29	L 29	Intel's 8251 description and interfacing with 8086	Class Room
30	L 30	Interrrupts and DMA: 8086 Interrupt mechanism; interrupt types and interrupt vector table.	Class Room
31	L 31	Applications of interrupts	Class Room
32	L 32	Intel's 8259	Class Room
33	L 33	DMA operation. Intel's 8237	Class Room