PANIPAT INSTITUTE OF ENGINEERING & TECHNOLOGY
Department of Electronics & Communication Engineering

LESSON PLAN

Subject Name: - Verilog HDL **Subject Code:** EC-306
Year: -3rd **Semester:-6th**

Lecture No	Unit No	Topic	COs Covered
L 1	Unit-I	Introduction to Verilog HDL, Conventional Approach to Digital Design	CO1
L 2		VLSI design, ASIC design flow, Role of HDL	
L 3		Conventional Data flow, ASIC data flow, Verilog as HDL	
L 4		Levels of Design Description, Concurrency, Simulation and Synthesis	
L 5		Functional Verification, System Tasks	
L 6		Programming Language Interface (PLI), Module	
L 7		Simulation and Synthesis Tools, Test Benches	
L 8		Introduction to Language constructs and conventions, Keywords, Identifiers, White Space Characters	
L 9		Comments, Numbers, Strings, Logic Values, Strengths, Data Types	
L 10		Scalars and Vectors, Parameters, Memory, Operators, System Tasks	
L 11		Revision	
L 12	Unit-II	Introduction to Gate level modelling, AND Gate Primitive, Module Structure	CO2
L 13		Other Gate Primitives, Illustrative Examples	
L 14		Tri-State Gates, Array of Instances of Primitives, Additional Examples	
L 15		Design of Flip-flops with Gate Primitives	
L 16		Delays, Strengths and Contention Resolution, Net Types	
L 17		Design of Basic Circuits	
L 18		Introduction to Behavioral Modelling, Operations and Assignments	
L 19		Functional Bifurcation, Initial Construct, Always Construct, Examples	
L 20		Assignments with Delays, Wait construct, Multiple Always Blocks	
L 21		Designs at Behavioral Level, Blocking and Non-blocking Assignments, The case statement	
L 22		Simulation Flow, if and if else constructs, assign-design construct	

L 23		repeat construct, for loop, disable construct	
L 24		while loop, forever loop, parallel blocks	
L 25		force-release construct, Event.	
L 26		Revisions	
L 27	Unit -III	Introduction to Modelling at data flow level, Continuous Assignment Structures	CO3
L 28		Delays and Continuous Assignments, Assignment to Vectors	
L 29		Operators, Additional Examples	
L 30		Bi-directional Gates, Time Delays with Switch Primitives	
L 31		Instantiations with Strengths and Delays, Strength Contention with Trireg Nets	
L 32		Revision	
L 33	Unit-IV	Function, Tasks	CO4
L 34		User- Defined Primitives (UDP)	
L 35		FSM Design (Moore and Mealy Machines).	
L 36		Introduction to System tasks, functions, and compiler directives, Parameters, Path Delays	
L 37		Module Parameters, System Tasks and Functions	
L 38		File-Based Tasks and Functions, Compiler Directives	
L 39		Hierarchical Access, General Observations	
L 40		Revision	

Text Books:

1. T. R. Padmanabhan, B. Bala Tripura Sundari (2004), Design through Verilog HDL, Wiley & SonsEducation, IEEE Press, USA.
2. J. Bhaskar (2003), A Verilog Primier, 2nd edition, BS Publications, India.

References:

1. Samir Palnitkar (2013), Verilog HDL, Pearson India.
2. Stephen. Brown, ZvonkoVranesic (2005), Fundamentals of Logic Design with Verilog, Tata McGraw Hill, India.
3. Charles H. Roth (2004), Digital Systems Design using VHDL, Jr. Thomson Publications, India.

Web resources:

1. https://onlinecourses.nptel.ac.in/noc21_ee97/preview